

RNA50C27AUS

CMOS System-Reset IC

REJ03D0834-0100 Preliminary Rev.1.00 Apr 10, 2006

Description

This IC facilitates complicated power-on and power-monitoring resets of microcomputers that require the 3.3-V and 1.8-V dual power supplies. It also facilitates change of delay time of reset signal by externally setting resistance and capacity for delay time. By employing complementary open-drain output, desired output such as open-drain output and CMOS output can be obtained.

Functions

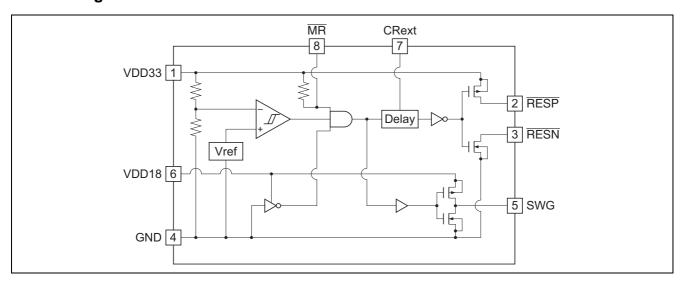
3.3-V detection voltage : 2.7 V
 Accuracy of 3.3-V detection voltage : ±1.0%
 Hysteresis of 3.3-V detection voltage : 5% Typ.

Open-drain/CMOS output

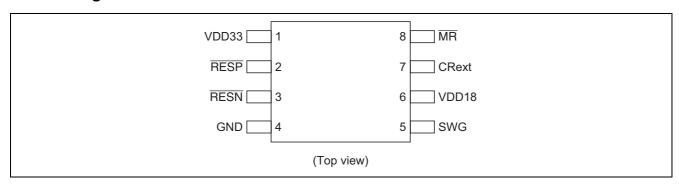
• 1.8-V PMOS drive output

• Ultra-small SSOP-8 package

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
1	VDD33	Input power supply pin for 3.3-V voltage. Recommended operating range is 2.7 to 3.6 V.
		Set the input voltage to 0.033 V/μs or less when starting up.
2	RESP	Active-low reset signal output pin. By connecting to RESN pin, CMOS output can be used.
		If using open-drain, please connect pull-down resistor.
3	RESN	Active-low reset signal output pin. By connecting to RESP pin, CMOS output can be used.
		If using open-drain, please connect pull-up resistor.
4	GND	GND pin
5	SWG	External PMOS gate control signal to be set between 1.8-V power supply and 1.8-V voltage
		input of microcomputer.
6	VDD18	Input power supply pin for 1.8-V voltage. Recommended operating range is 1.65 to 3.6 V.
7	CRext	Connecting pin for Rext resistance and Cext capacity that determine the delay time of reset
		signal.
		$3.3~k\Omega$ or more is recommended for resistance. The delay time, t_{DLY} , is given by the
		following formula.
		$t_{DLY} = Cext \times Rext[s]$
8	MR	Pin to provide reset manually. MR pin is pulled-up to VDD33 through internal resistor.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	VDD33	4.6	V
	VDD18	4.6	
Input voltage	V _I	-0.3 to VDD33+0.3	V
Output voltage	Vo	-0.3 to VDD33+0.3	V
Input current	I _I	20	mA
Output current	Io	25	mA
Supply current	I _{DD}	25	mA
Power dissipation	P _T	273	mW
Storage temperature	Tstg	-55 to +125	°C

Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit	Remarks
Supply voltage	VDD33	VTH33	_	3.6	V	
	VDD18	1.65	_	VDD33		
Input voltage	V_{MR}	0	_	VDD33	V	
Output voltage	Vo	0	_	VDD33	V	
	Voswg	0	_	VDD18		
External resistor	Rext	3.3	_	_	kΩ	VDD33 = 3.3 V
External capacitor	Cext	_	No limit	_		
Drivable capacitor	CL	_	2200	_	pF	SWG output
Operating temperature	Та	-40	_	85	°C	

Electrical Characteristics

DC Characteristics

 $(VDD33 = 3.3 \text{ V}, VDD18 = 1.8 \text{ V}, Ta = 25^{\circ}\text{C}, CRext:R = 10 \text{ k}\Omega)$

ltem		Symbol	Min	Тур	Max	Unit	Test Conditions
Quiescent supply current		IDD33	0.75	1.5	4	μΑ	All outputs are open
		IDD18	0.25	0.5	2		
Detectio	n voltage	VTH33	Typ×0.99	2.7	Typ×1.01	V	
		VTH _H	1.2	_	_		
		VTH∟	_	_	0.55		
	Detection voltage temperature dependency		_	±100	_	ppm/°C	
Detectio	Detection voltage hysteresis		VTH33×3%	VTH33×5%	VTH33×8%	V	
MR	Low-level input voltage	V _{IL}	_	_	VTH33×0.25	V	
	High-level input voltage	V _{IH}	VTH33×0.75	_	_	V	
	internal pull-up resistance	R _{MR}	_	T.B.D.	_	kΩ	
CMOS	Low-level output current	I _{OL}	7.5	15	30	mA	V _O = 0.5 V
*1	High-level output current	I _{OH}	5	10	20		$V_0 = VDD33 - 0.5 V$
RESP	Output leakage current	I _{LEAK}	_	_	0.1	μΑ	RESN off
RESN	Output leakage current	I _{LEAK}	_	_	0.1	μΑ	RESP off
SWG	High-level output voltage	V _{OH}	1.7	_	_	V	V _O = open
	Output source current	Іон	1.5	3	6	mA	V _O = VDD33 - 0.5 V
	Low-level output voltage	V _{OL}			0.1	V	V _O = open
	Output sink current	I _{OL}	0.2	0.35	0.55	mA	V _O = 0.5 V

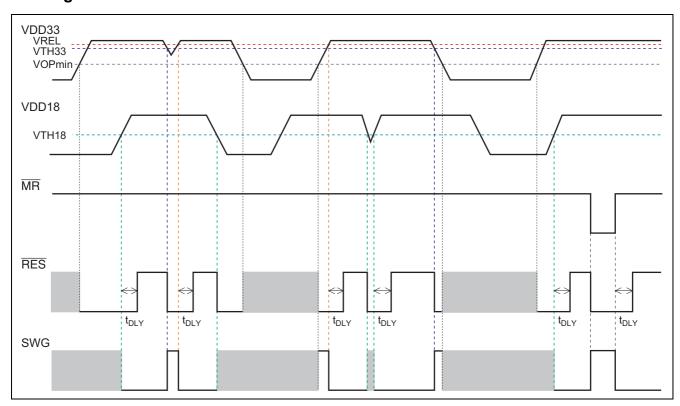
Note: When the voltage within $V_{IL} < V_{IN} < V_{IH}$ is applied to MR and VDD18 input by DC, oscillation may occur.

AC Characteristics

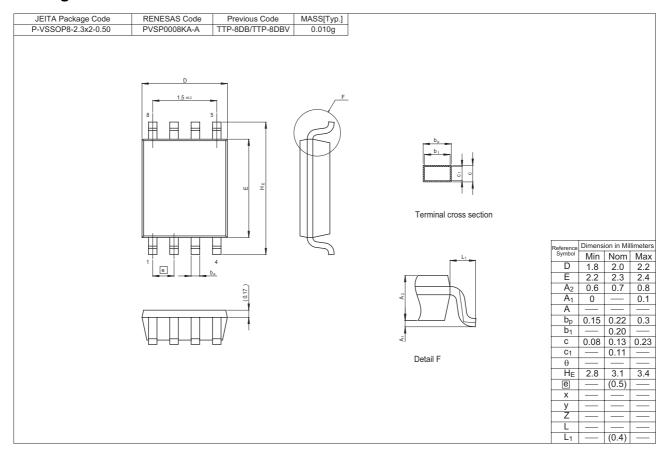
Item		Symbol	Min	Тур	Max	Unit	Test Conditions
RESP	Propagation delay time	tp _{LH}	_	50	400	μs	$C_L = 15 pF$,
		tp _{HL}	_	5	T.B.D.		CRext:C = open
	Response time	t _r	_	5	T.B.D.	ns	C _L = 15 pF
		t _f	_	5	T.B.D.	μs	
RESN	Propagation delay time	tp _{LH}	_	50	400	μs	$C_L = 15 \text{ pF},$
		tp _{HL}	_	1.5	T.B.D.		CRext:C = open
	Response time	t _r	_	5	T.B.D.	μs	C _L = 15 pF
		t _f	_	5	T.B.D.	ns	
SWG	Propagation delay time	tp _{LH}	_	50	400	μs	C _L = 2200 pF
		tp _{HL}	T.B.D.	1.5	T.B.D.		
	Response time	t _r	T.B.D.	1.0	T.B.D.	μs	
		t _f	T.B.D.	7.6	T.B.D.		
Delay time		t _{DLY}	_	93	_	ms	CRext:C = 0.1 μ F, R = 1 M Ω

^{1.} When RESP output and RESN short out and CMOS output is used.

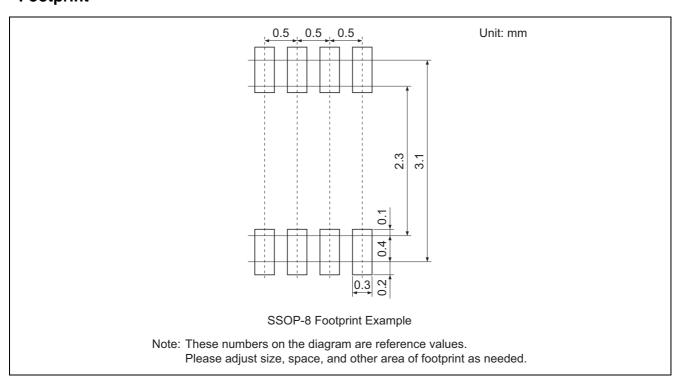
Timing Chart



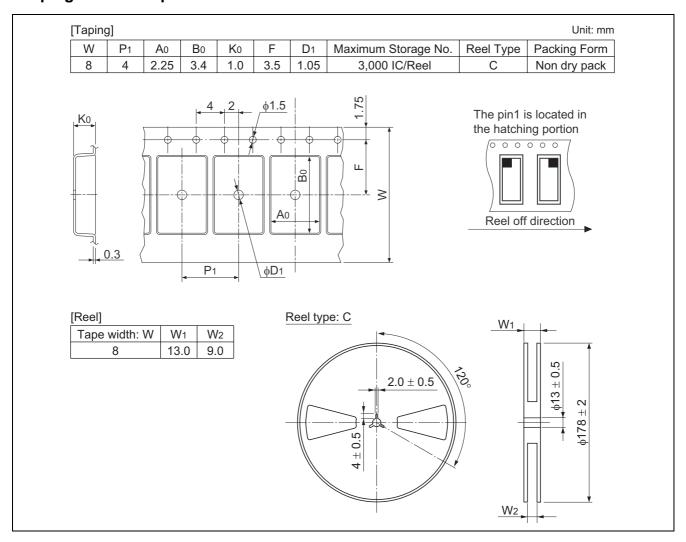
Package Dimensions



Footprint



Taping and Reel Specifications



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